RECEIVED
CENTRAL FAX CENTER
JAN 04 2007

Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to clarify Applicants invention. No new matter has been added.

For example support for the amendments is found in the previously presented claims Figures 1D, 1E and Figure 2 and in the Specification at:

Paragraph 0030

> The present invention contemplates an ESD-resistant photomask for transferring a circuit pattern onto a photoresist layer provided on a semiconductor wafer during the photolithography stage of integrated circuit fabrication. The ESD-resistant photomask includes a transparent mask substrate, a pattern-forming material deposited on the substrate, **light-transmissive exposure regions** etched in the pattern-forming material to define a circuit pattern, and positive or negative ions implanted into the substrate throughout ion implantation regions which typically span the exposure regions in the mask. Electrostatic charges on the mask are dissipated by the ions in the ion implantation regions, thus preventing the buildup of electrostatic charges which could otherwise attract image-distorting particles to the mask or damage the mask.

Claim Rejections under 35 USC 103

1. Claims 1-20 stand rejected under 35 USC 103(a) as being unpatentable over Levinson et al. (US 6, 984,475) in vies of Ker

et al. (US PUB 20050051848) or Hsu (US 5,585,299).

Levinson et al. disclose an extreme ultraviolet (EUV) lithography mask including structural features to facilitate indirect electrical grounding of a reflector film on the frontside of the mask **to remove electrical charge generated during EUV light exposure in an EUV lithography system** (see Abstract; col 3, lines 25-39; col 4, lines 59-col 5, lines 4; col 8, line 64-col 9, line 4). The EUV mask of Levinson et al. facilitates electrical grounding of the EUV mask and overcomes the problem of the electrical charging of the mask caused by generation of photoelectrons on the front side of the mask (including reflector/absorber films) (28; Figure 3) by incident EUV energy (26), where the electrical charge generated on the frontside of the mask may cause particle attraction or electrostatic discharge damage to the mask (col 4, lines 51-59). Electrical grounding of the mask (see Fig6ures 4, 5, 8-10) during EUV irradiation **removes (to ground) the excess charge generated** in the mask during EUV irradiation (col 6, line 57-col 7, line 2).

Levinson et al. discloses several structural features for facilitating indirect grounding of the frontside of the mask

including forming a conducting layer (46; Figures 4 and 5) on the bottom surface (backside) of the mask which connects with the frontside reflector film (64); encapsulating the substrate with a conductive layer (100; Figure 8); forming a thinned region (114; Figure 9) from the backside of the substrate so that a conductive layer (118) and the reflector layers (120) are interconnected by a doped conductive region (116) formed in the substrate; and by forming a hole (138/140; Figure 10) filled or lined with a conductive material through the substrate to connect the conductive layer (134) to the reflector layers (136).

Levinson et al. teaches that in the embodiment where a the backside of the substrate is thinned to form a recess where the thinned area of the substrate (116; Figure 9) is impregnated or implanted with dopant ions to increase conductivity of the substrate (see col 9, lines 16-39), that **the thinned portion** is preferably located adjacent **a periphery of the substrate** to avoid **introducing distortions in the EUV reflected pattern generated by the mask** (col 9, lines 35-39).

The grounding is accomplished through mechanical means such as probes (col 5, lines 36-44; col 7, lines 43-55; col 7, lines 43-55) where the grounding has the effect of avoiding the

attraction of particles to the frontside reflector/absorber film and to dissipate charge generated in the mask to ground.

In contrast, Ker discloses a method for forming ion **implanted source and drain regions** including implanting ions underneath source and drain regions **to provide ESD protection in an ESD circuit** (see Abstract).

In further contrast Hsu discloses a method for forming an ESD protection circuit where both dual diffusion source/drain FETs (ESD protection region) as well as lightly doped (LDD) transistors (functional regions) are used, and where the ESD capability of the LDD transistor is enhanced by using the same mask to form more heavily doped regions (underlying/encompassing the source drain regions) in both regions of the substrate (see col 1, lines 15-24; lines 38-49; col 2, lines 1-7; col 4, lines 53-64).

Even assuming *arguendo* that Hsu or Ker are analogous art, and even assuming *arguendo* a proper motivation for combining the disparate teachings of forming an ESD circuit (Ker and Hsu) and an EUV photomask (Levinson), such combination does not produce Applicants disclosed and claimed invention includdingthe

following portions in **bold type**.

"A method of preventing electrostatic discharge damage to a photomask, comprising the steps of:

providing a mask substrate;

providing a pattern-forming material on said mask substrate;

providing patterned **light-transmissive** exposure regions in said pattern-forming material; and

providing at least one ion implantation region in said mask substrate by implanting ions into said mask substrate, **wherein said at least one ion implantation region comprises at least one of said patterned light-transmissive exposure regions.**"

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

The cited references, individually or in combination, fail to produce or suggest Applicants invention and are therefore insufficient to make out a *prima facie* case of obviousness with respect to Applicants disclosed and claimed invention.

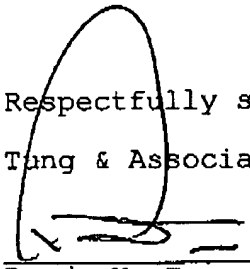
The claims have been amended to further clarify Applicants' disclosed and claimed invention. A favorable consideration of Applicants' claims is respectfully requested.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

Tung & Associates



Randy W. Tung
Reg. No. 31,311
Telephone: (248) 540-4040